On-Board Probing of Broadband RF Amplifiers Using CPW Interconnects

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***Abstract*: Printed circuit boards with edge-connectors for insertion into appropriate sockets on a mother-board are used in the RF industry as functional circuit blocks. For example, RF amplifiers in high-speed data transmission, video communication and broadband cable television systems employ modular interconnect circuit boards for attenuation, matching, etc. This paper presents a novel method for the on-board (*in-situ*) characterization of interstage functional blocks in broadband RF amplifiers, utilizing CPW plug-in connectors. We discuss an on-board calibration technique to compensate for the connector mismatch, and present measured data useful in modeling broadband high-power RF circuitry.**

I. INTRODUCTION

The increasing commercial use of RF integrated circuits in communications, computing and cable television industries requires accurate probing methods to measure the performance of printed circuit boards. Like their digital counterparts, RF systems employ modular interconnect boards for circuit functions such as attenuation, matching, filtering, etc., to save substrate real estate on the mother-board and facilitate plug-and-play convenience. Test equipment manufacturers recognized the need for automated testing of printed circuit boards and found that by using properly calibrated measurements with test probes, one can achieve a moderate success in detecting board failures. Examples of commercially available in-circuit probes are the K-50 probe made by a collaborative arrangement between Motorola and Everett Charles Technologies [1], [2] and the SWD switchable connector manufactured by Murata [3]. However, these probes are not useful in applications where the probe and the motherboard interface through an edge connector or a pin-socket interface.

This paper presents a novel method for the on-board (*in-situ*) measurement of interstage functional blocks in broadband RF amplifiers, using coplanar waveguide (CPW) interconnect boards with pin-socket connectors. The physical nature of the pin-socket interface is such that accurate field analysis, required for its RF characterization, can be gained only from full-wave 3D simulation (using FEM for example). Because of the complexity and the variety of functional plug-in cards used in practice, 3D simulation is of limited practical value. Therefore, we have developed plug-in boards to measure RF signals along any path in a broadband high-gain amplifier, with access to pin-socket ports. We have developed on-board calibration procedures, which compensate for the probe parasitics, and place the reference plane close to the probe-tip. Thus, S-parameters on a printed circuit trace can be directly measured using a Vector Network Analyzer (NA). A set of board calibration standards has been designed to compensate for the errors associated with the measurement path.

We have evaluated the accuracy of these probes and the calibration process in two steps. First, we perform calibrated S-parameter measurements of individual two-port blocks in the RF amplifier, which have the plug-in pin-socket interface at each port location. Next, we cascade the T-matrices of all these blocks and compare the result with the overall unit measurement between the input and the output connectors of the amplifier. Magnitude discrepancy less than 0.5dB and phase discrepancy less than a few degrees in the S-parameters confirm the accuracy of the probe characterization and the on-board measurement procedure. It is anticipated that such characterization of the probes will be very useful to develop circuit models for the associated circuit stages from measured data.

II. MEASUREMENT AND CALIBRATION

A. Board Calibration Standards

For a given pin and socket configuration, we have designed calibration standards comprising a distributed open, short, 75 ohm precision load and thru line, in a grounded coplanar waveguide (GCPW) transmission environment. These standards replace the standard N-type

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coaxial calibration standards supplied with the HP 8753E Network Analyzer. Because these are application-specific calibration terminations, we need to enter the calibration constants for these manually and do a "user calibration" on the Network Analyzer, as described in [4] and [5]. The calibration standards are all fabricated on a single board and mounted in a metal fixture with N-connector feeds to the NA. The footprint layout of a typical calibration board, used for SMD components, is shown in Fig. 1.

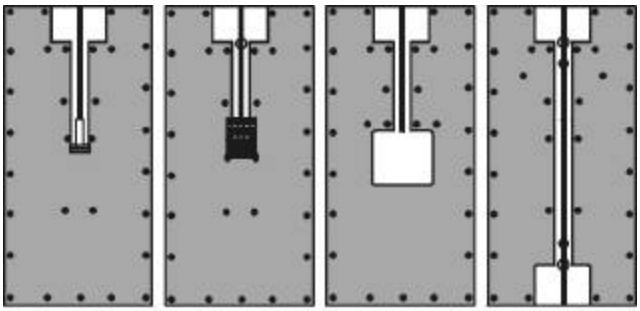

Fig. 1. Layout of on-board calibration standards to establish the reference planes at the edges of the probe-tip. (a) Load, (b) Short, (c) Open, and (d) Thru.

B. User Calibration

We have designed four precision standards, Short, Open, Load and Thru (SOLT) (see Fig. 1), for 12-term error correction at the board reference planes [4], [5]. The load and thru are of zero length offset and 75 ohm impedance. A precision broadband chip resistor of 75 W was connected at the reference plane for the load standard. An ideal open circuit is impossible. The non-ideal open (Fig. 1) presents fringe capacitance at the end, which needs to be calculated as a function of frequency for input to the NA. This capacitance is measured as follows. First, we perform a one-port calibration at the input N-connector using the standard N-connector calibration kit. Then we connect the board calibration standard, *Short* (see Fig. 1), and using the port extension feature of the NA [5], we roll the N-connector reference plane to the end of the *Short*. This operation essentially compensates for the phase delay between the two reference planes. Next, we replace the board *Short* with the board *Open*, and with the Input Port Extension *ON*, we measure the input reflection coefficient, S_{11}. The input impedance at the reference plane of the open is given by

$$Z_{in} = R_{op} + jX_{op} = Z_c \frac{1+S_{11}}{1-S_{11}} \qquad (1)$$

where $Z_c = 75$ W. The fringe capacitance of the open circuit follows from

$$C_{op} = -\frac{1}{2p\, fX_{op}} \qquad (2)$$

This measured capacitance shows frequency dependence because of dispersion of the open-circuit. The frequency dependence is incorporated by fitting the measured data to a polynomial of the form

$$C(f) = C_0 + C_1 f + C_2 f^2 + C_3 f^3 \qquad (3)$$

The constants C_0 L C_3 are input to the NA as calibration constants for the board *Open* standard. All the calibration constants for the four standards in Fig. 1 are recorded and stored in the NA's internal memory.

C. Measurement

After calibration, the RF amplifier, a 2-stage power amplifier with about 35 dB gain between 100 MHz and 1 GHz, is connected to the NA, proper bias is applied, and the input power is adjusted so that the amplifier operates below the compression point. The circuit contains two Si power doubler ICs (gain blocks or hybrids), with each having 40 dB maximum available gain. At the input and in between the two stages, we have equalizers to compensate for amplitude distortion along the path. The input and output amplifier hybrids are preceded by matching networks. The S-parameters are measured using the probe connected to the appropriate plug-in port.

III. MEASUREMENT EXAMPLE

Fig. 2 displays the block schematic of a typical amplifier. The first sketch denotes measurement (i.e., a measured two-port S-parameter file) from the input connector to the output connector. The second sketch denotes a three-block cascade, with the circuit broken at the input and the output terminals of an interstage attenuator pad. The pad is designed to provide gain adjustment. Thus, the first block represents circuit measurement between amplifier input and the pad, the second block represents measurement of the pad itself, and the third corresponds to measured circuit between the pad and the amplifier output. The first and third blocks contain amplifier hybrids, while the second is entirely passive.

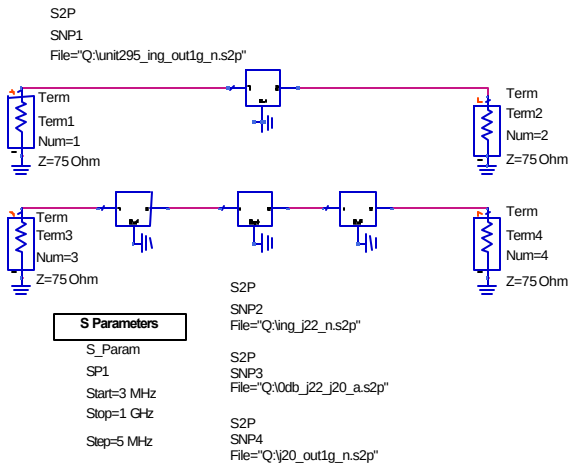

Fig. 2. A three-block ADS cascade model of the RF amplifier.

Fig. 3 compares magnitude and phase of S11 between the measured cascade model and the overall unit measurement. The agreement in magnitude is within 0.2 dB and the phase discrepancy is less than 0.5 deg. The return loss is less than 18 dB over the desired frequency range and agrees with the specifications.

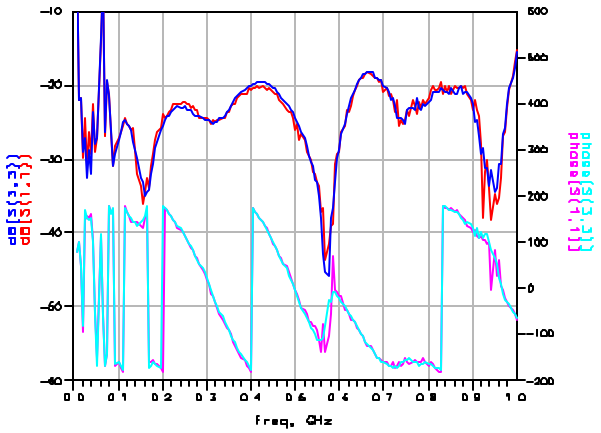

Fig. 3. Comparison between overall unit measurement and the cascade measured model for S11.

Fig. 4 likewise compares the magnitude and phase of S21, with good corroboration observed between the cascade and the unit measurements. The gain of more than 34 dB is realized between 100 MHz and 1 GHz. This corroboration validates the accuracy of the on-board calibration and S-parameter probing of PCBs using the CPW interconnect cards. The error analysis presented next quantifies the maximum measurement error.

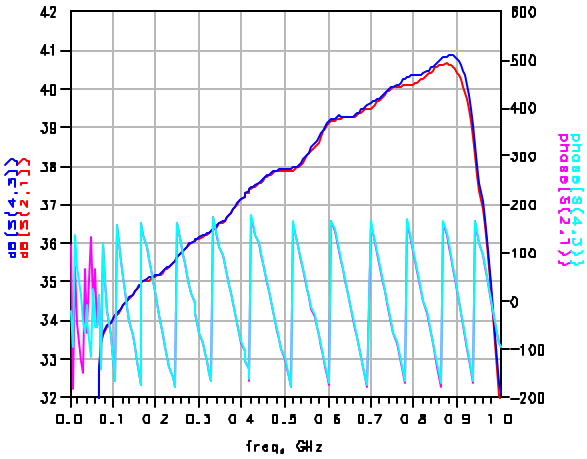

Fig. 4. Comparison between overall unit measurement and the cascade measured model for S21.

IV. Measurement Error

In order to study the repeatability of the probes and quantify the measurement error, we have measured S-parameters of the *same unit* from the input of the amplifier to the first hybrid, fifteen times, by randomizing the calibration and measurement sequence. All other variables such as cables and adapters were unchanged. This circuit block does not contain the amplifier ICs, and thus we need not drive the input too low (an input power of -10 dBm is used for the NA).

Fig. 5 shows the S11 magnitude for the 15 measurements. From this data, we calculate the *repeatability limit*, defined as the maximum absolute difference that approximately 95% of all pairs of replications under the same test conditions should be less than [6]. Since the differences assume a normal distribution, using probability theory, we calculate the repeatability limit as $rl = 2.77\boldsymbol{s}_e$ where $\boldsymbol{s}_e$ is the S11 standard deviation at a given frequency.

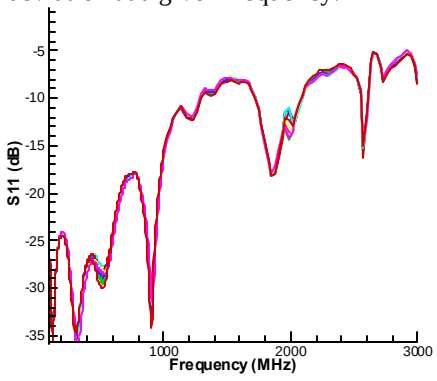

Fig. 5 Repeatability of S11 measurements on a passive circuit.

From Fig. 5, we calculate the measurement repeatability to be within about 0.5 dB, comparable to the measurement uncertainty of the NA. The repeatablity of S21, not shown for brevity, was better than 0.5 dB.

Fig. 6 plots the standard deviation (SD) of the fifteen S11 magnitude measurements, calculated at each frequency. The standard error (SE), defined as $SD/\sqrt{N}$, where $N = 15$ is the number of measurements, gives an estimate of the measurement error. Thus, two-sided error bars can be visualized at each frequency, with an absolute error of $Data \pm SE$ in units of the measured variable. From Fig. 6, we determine that the maximum magnitude error in S11 is $1.5/\sqrt{15} = 0.4$ dB.

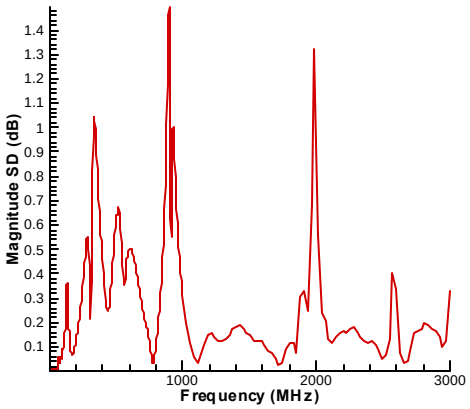

Fig. 6. Standard deviation in magnitude of S11.

Likewise, the maximum error in S11 phase, computed from the standard deviation plotted in Fig. 7, is about 2.3 degrees. The maximum magnitude and phase errors in S21 measurement are calculated as 0.5 dB and 3.5 degrees, respectively. These errors appear to be within the error margin of the 8753 Network Analyzer measurements [5].

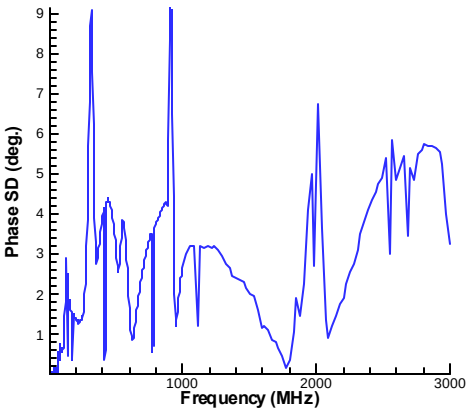

Fig. 7. Standard deviation in phase of S11.

V. Conclusion

We have presented a novel method for the on-board (*in-situ*) measurement of interstage functional blocks in broadband RF amplifiers, using coplanar waveguide interconnect boards with pin-socket connectors. Besides providing measured data to model various sections of a large circuit, a truly practical application for such probing is to diagnose the circuit performance at various points of the circuit where socket configuration appropriate to the probe is available on the motherboard. In fact, such sockets can also be used to provide test points for automated testing of the circuit. With appropriate modification, the proposed method also applies to block-deembedding of circuits with edge connector ports. In fact, using measured data, one can develop circuit models for complicated circuit blocks, which are inevitably impractical to model using simulations alone.

Acknowledgement

The author acknowledges the support of Engineering Managers Paul Romanowski and Dave Thibado at the RF R&D Division of Philips Broadband Networks, during various phases of this work.

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